WHAT IS CLAIMED IS:

1. A MOSFET structure comprising:

a substrate;

a tortuous gate on the substrate;

a gate dielectric layer between the tortuous gate line and the substrate; and

a source region and a drain region in the substrate beside the tortuous gate line, wherein the source region has a broader part and a narrower part, and the drain region has a broader part and a narrower part, wherein the broader part of the source region is disposed opposite to the narrower part of the drain region and the narrower part of the source region is disposed opposite to the broader part of the drain region.

2. The MOSFET structure of claim 1, wherein at least a contact is disposed on the broader part of the source region and at least a contact is disposed on a broader part of the drain region.

3. The MOSFET structure of claim 1, wherein the material of the tortuous gate line comprises doped polysilicon.

4. A MOSFET structure comprising:

a substrate;

a tortuous gate on the substrate;

a gate dielectric layer between the tortuous gate and the substrate;

a source region and a drain region disposed within the substrate adjacent to the tortuous gate, wherein the source region has a broader part and a narrower part, and the drain region has a broader part and a narrower part, wherein the broader part of the source region is disposed opposite to the narrower part of the drain region, and the

narrower part of the source region is disposed opposite to the broader part of the drain region; and

a metal-silicide layer disposed on the tortuous gate and on the source and drain regions.

5. The MOSFET structure of claim 4, wherein at least a contact is disposed on the broader part of the source region and at least a contact is disposed on a broader part of the drain region.

6. The MOSFET structure of claim 4, wherein the material of the tortuous gate line comprises doped polysilicon.

7. The MOSFET structure of claim 4, wherein the material of the metal-silicide layer is selected from the group comprising titanium silicide, cobalt silicide, nickel silicide, and palladium silicide.

8. A metal oxide semiconductor device comprising:

a substrate;

a tortuous gate on the substrate;

a gate dielectric layer between the tortuous gate and the substrate;

a lightly doped source region, a source region, a lightly doped drain region, and a drain region disposed within the substrate located adjacent to the tortuous gate line, wherein the lightly doped source region, the source region, the lightly doped drain region, and the drain region have a broader part and a narrower part, respectively, wherein the broader part of the lightly doped source region / source region is opposite to the narrower part of the lightly doped drain region / drain region, and the narrower part of the lightly doped source region / source region is opposite to the broader part of the lightly doped drain region / drain region; and

a first metal silicide layer disposed on the tortuous gate and a second metal silicide layer disposed on the source and drain regions.

9. The metal oxide semiconductor device of claim 8, wherein at least a contact is disposed on the broader part of the source region and at least a contact is disposed on a broader part of the drain region.

10. The metal oxide semiconductor device of claim 8, wherein the material of the gate comprises doped polysilicon.

11. The metal oxide semiconductor device of claim 8, wherein the material of the first metal-silicide layer is selected from one of the group comprising titanium silicide, cobalt silicide, nickel silicide, and palladium silicide.

12. The metal oxide semiconductor device of claim 8, wherein the material of the second metal-silicide layer is selected from one of the group comprising titanium silicide, cobalt silicide, nickel silicide, and palladium silicide.

13. The metal oxide semiconductor device of claim 8, wherein the material of the first metal-silicide layer on the tortuous gate and the material of the second metal silicide layer of the source/drain regions are substantially of same material.

14. The metal oxide semiconductor device of claim 8, wherein the material of the first metal-silicide layer on the tortuous gate is different from that of the second metal-silicide layer on the source/drain region.

15. The metal oxide semiconductor device of claim 8, wherein the material of the first metal-silicide layer is titanium silicide.

16. The metal oxide semiconductor device of claim 8, wherein the material of the second metal-silicide layer on the source/drain region is titanium silicide.

17. A metal oxide semiconductor device comprising:

a tortuous gate line on the substrate;

a gate dielectric layer between the tortuous gate line and the substrate; and

a lightly doped source region, a source region, a lightly doped drain region, and a drain region disposed within the substrate located adjacent to the tortuous gate, wherein the lightly doped source region, the source region, the lightly doped drain region, and the drain region have a broader part and a narrower part, respectively, wherein the narrower part of the lightly doped source region / source region is opposite to the broader part of the lightly doped drain region / drain region, and the broader part of the lightly doped source region / source region is opposed to the narrower part of the lightly doped drain region / drain region.

18. The metal oxide semiconductor device of claim 17, wherein at least a contact is disposed on the broader part of the source region and at least a contact is disposed on a broader part of the drain region.

19. The metal oxide semiconductor device of claim 17, wherein the material of the gate line comprises doped polysilicon.